Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Previously Presented) A method for processing data using a plurality of processing engines, the method comprising:

processing first data associated with a first control record in a first processing engine;

processing second data associated with a second control record in a second processing engine, wherein the first and second data are processed in parallel;

if processing of the first data completes before processing of the second data completes and the first control record is younger than the second control record, moving a first interrupt indicator associated with the first control record onto a second interrupt indicator associated with the second control record, wherein moving the first interrupt indicator comprises setting the first interrupt indicator associated with the first control record to disabled and setting the second interrupt indicator associated with the second control record to enabled; and

if processing of the first data completes before processing of the second data completes and the first control record is older than the second control record, generating an interrupt when processing of the first data completes, the interrupt being generated before processing of the second data completes.

2. (Original) The method of claim 1, wherein the first processing engine is a public key engine.

3. (Previously Presented) The method of claim 1, wherein moving the first interrupt indicator comprises determining that the first interrupt indicator is enabled.

4. (Previously Presented) The method of claim 1, wherein moving the first interrupt indicator comprises delaying the generation of an interrupt associated with the first control record.

5-7. (Cancelled)

8. (Previously Presented) The method of claim 1, wherein the first control record comprises a reference to data.

9. (Previously Presented) The method of claim 8, wherein the first control record comprises a reference to an operation to be performed on data.

10. (Original) The method of claim 1, further comprising writing processed data to memory associated with a host.

11. (Previously Presented) The method of claim 10, wherein the host is an external processor coupled to the processing engines.

12. (Previously Presented) The method of claim 11, wherein the external processor is coupled to the processing engines through a scheduler.

13. (Cancelled)

14. (Previously Presented) The method of claim 12, wherein the external processor reads the processed data when the interrupt is generated.

15. (Current Amended) A cryptography accelerator, comprising:

a first processing engine configured to process a first control record;

a second processing engine configured to process a second control record, wherein the first and second processing engines are configured to process the first and second control records in parallel;

a history buffer configured to retain information associated with the first and second control records including a first interrupt indicator associated with the first control record and a second interrupt indicator associated with the second control record;

wherein the ~~history buffer is configured to move~~ the first interrupt indicator associated with the first control record <u>is moved</u> onto a second interrupt indicator associated with the second control record if processing of the first control record completes before processing of the second control record completes and the first control record is younger than the second control record; and

wherein an interrupt is ~~configured to be~~ generated if processing of the first control record completes before processing of the second control record completes and the first control record is older than the second control record, the interrupt configured to be generated before processing of the second control record completes.

wherein moving the first interrupt indicator comprises setting the first interrupt indicator associated with the first control record to disabled and setting the second interrupt indicator associated with the second control record to enabled.

16. (Original) The cryptography accelerator of claim 15, wherein the first processing engine is a public key engine.

17. (Cancelled)

18. (Previously Presented) The cryptography accelerator of claim 15, wherein moving the first interrupt indicator associated with the first control record onto the second control record further comprises delaying the generation of an interrupt associated with the first control record.

19-21. (Cancelled)

22. (Original) The cryptography accelerator of claim 15, wherein the second control record comprises a reference to data.

23. (Original) The cryptography accelerator of claim 22, wherein the second control record comprises a reference to an operation to be performed on data.

24. (Previously Presented) The cryptography accelerator of claim 23, further comprising an external processor coupled to the processing engines through a scheduler.

25. (Cancelled)

26. (Previously Presented) The cryptography accelerator of claim 24, wherein the external processor reads the processed data when the interrupt is generated.

27-43. (Cancelled)